FIGURE 1

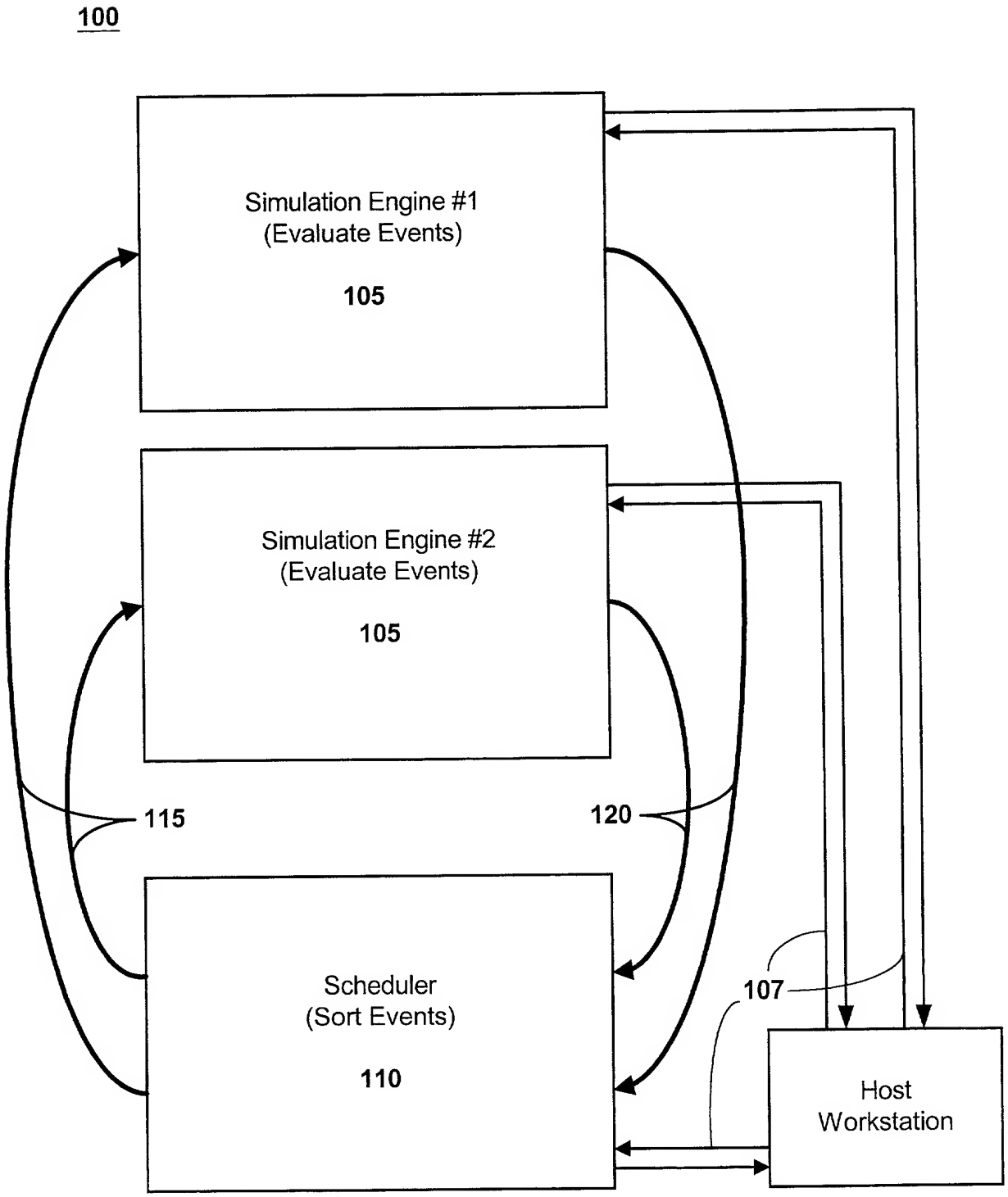

100
Simulation Engine #1
(Evaluate Events)
105
Simulation Engine #2
(Evaluate Events)
105
115
120
Scheduler
(Sort Events)
110
107
Host
Workstation

FIGURE 2

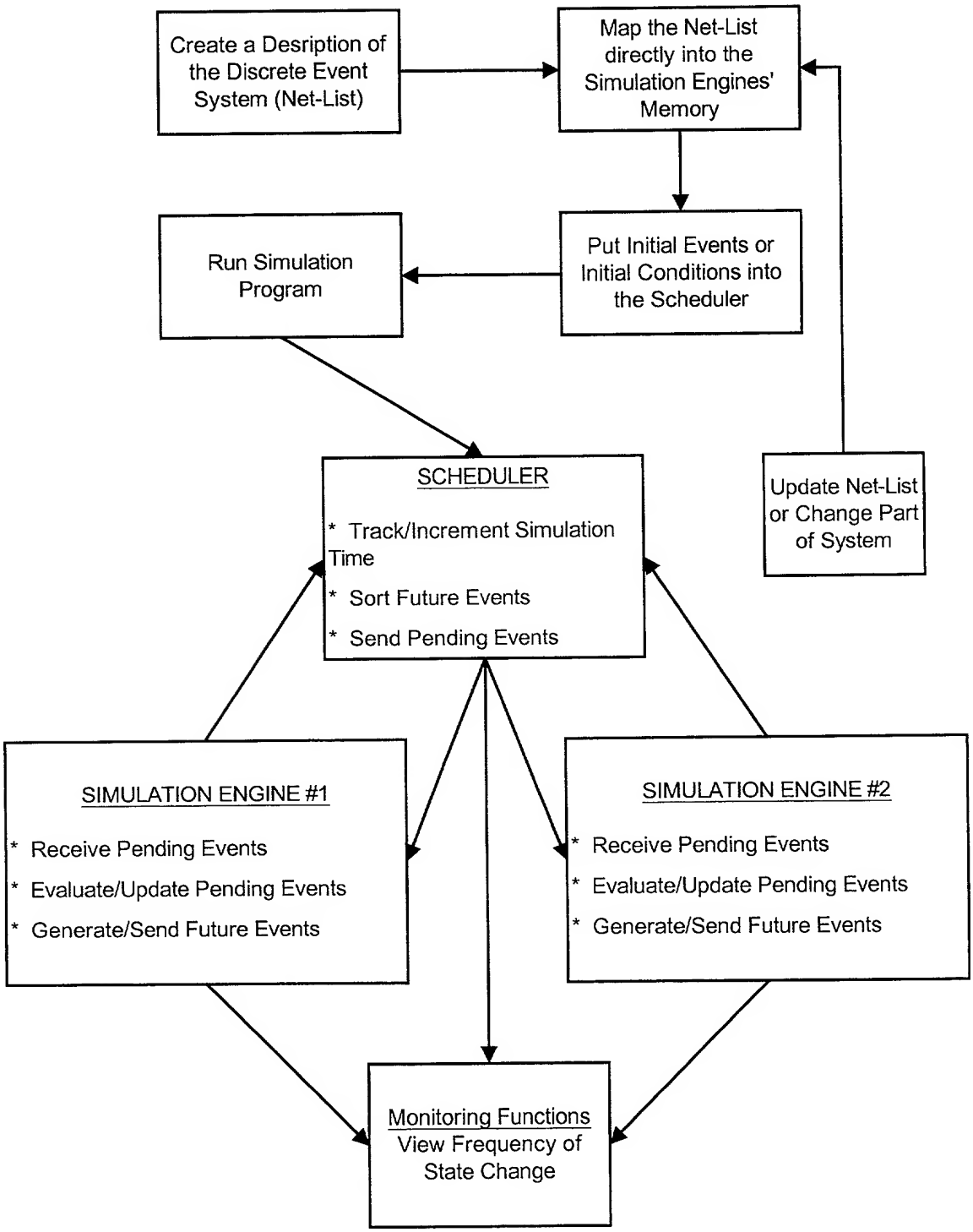

Create a Desription of the Discrete Event System (Net-List)
Map the Net-List directly into the Simulation Engines' Memory
Put Initial Events or Initial Conditions into the Scheduler
Run Simulation Program
SCHEDULER
* Track/Increment Simulation Time
* Sort Future Events
* Send Pending Events
Update Net-List or Change Part of System
SIMULATION ENGINE #1
* Receive Pending Events
* Evaluate/Update Pending Events
* Generate/Send Future Events
SIMULATION ENGINE #2
* Receive Pending Events
* Evaluate/Update Pending Events
* Generate/Send Future Events
Monitoring Functions
View Frequency of State Change

FIGURE 3

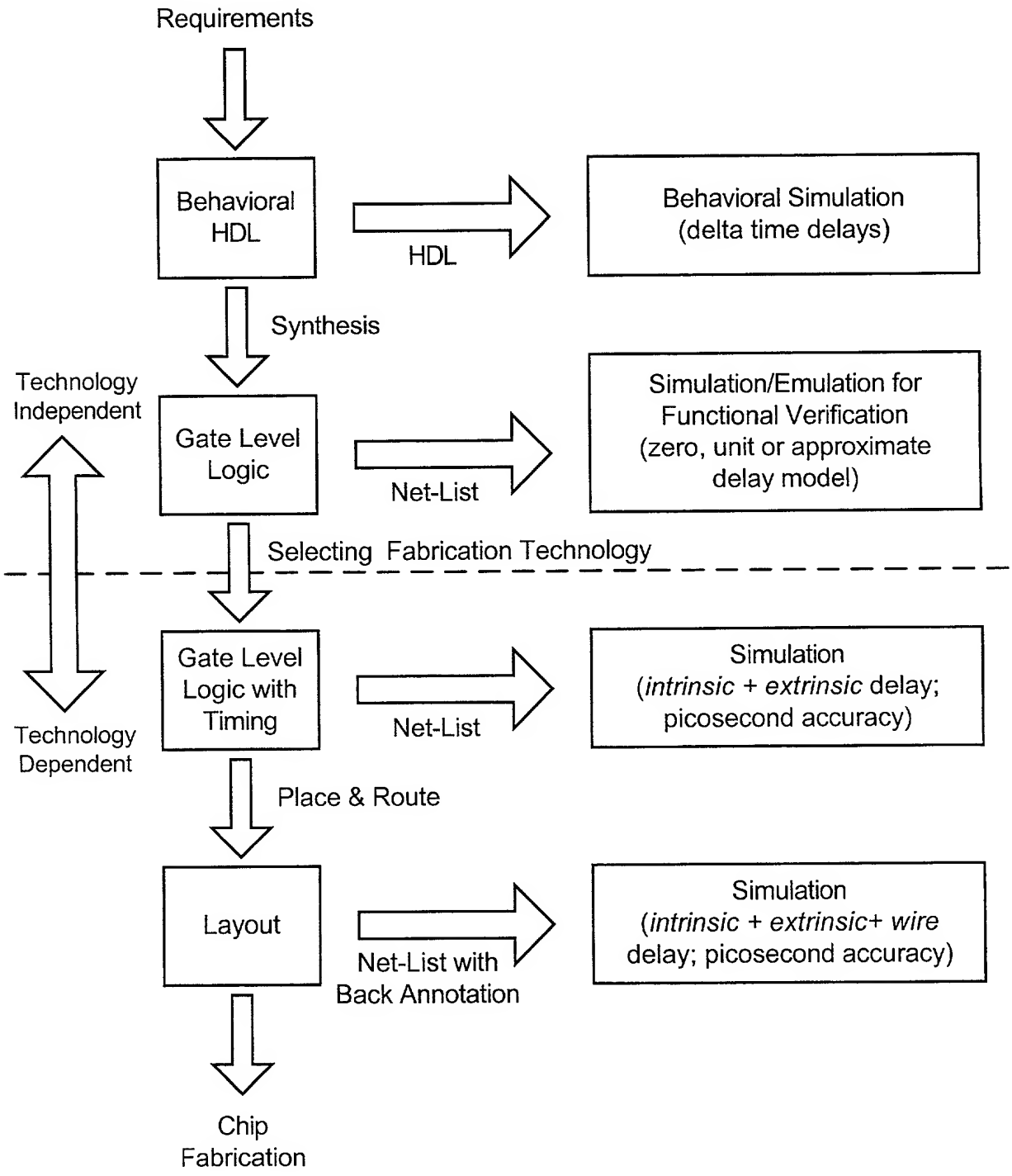
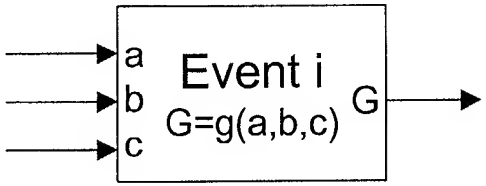

Requirements
Behavioral HDL
HDL
Behavioral Simulation (delta time delays)
Synthesis
Technology Independent
Gate Level Logic
Net-List
Simulation/Emulation for Functional Verification (zero, unit or approximate delay model)
Selecting Fabrication Technology
Gate Level Logic with Timing
Net-List
Simulation (intrinsic + extrinsic delay; picosecond accuracy)
Technology Dependent
Place & Route
Layout
Net-List with Back Annotation
Simulation (intrinsic + extrinsic+ wire delay; picosecond accuracy)
Chip Fabrication

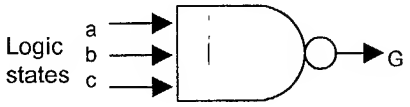
Figure 4A

Generalized Model



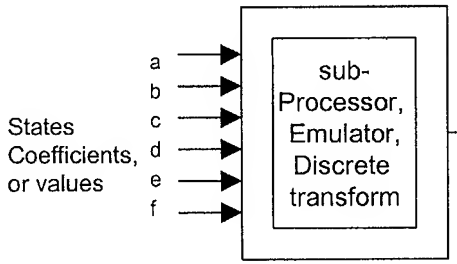
Particular inputs a,b,c cause an event #i at output G

Example Scenario Cases:



Digital Logic
"NAND Gate" &
Fanout connections

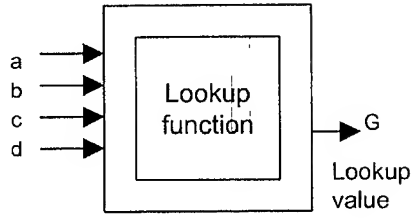
Logic Gate
Simulation



{within +/-limits,
distance moved,
pass/fail, etc.}

Mechanical,
Molecular,
Physical Simulation

Lookup, Matrix,
Algebraic
Simulation



Lookup
value

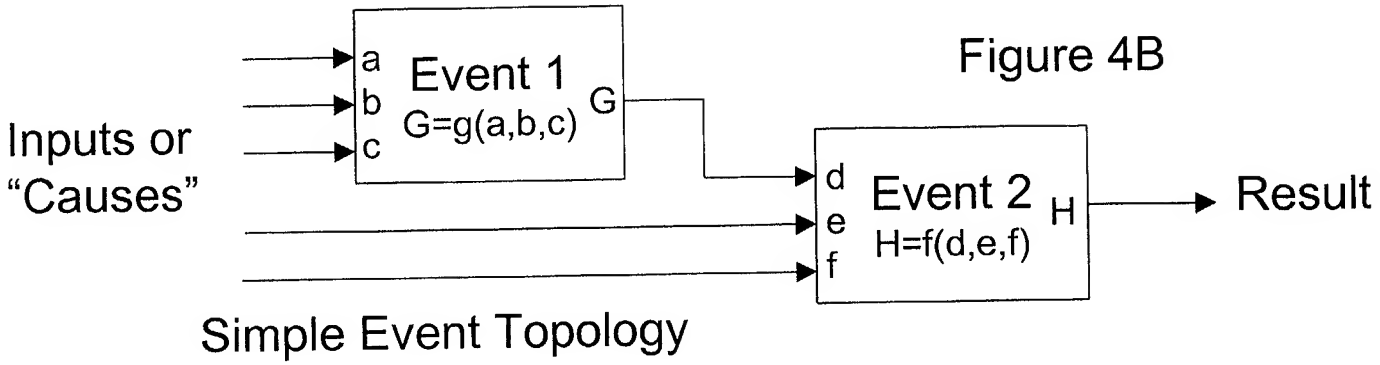


Figure 4B

Simple Event Topology

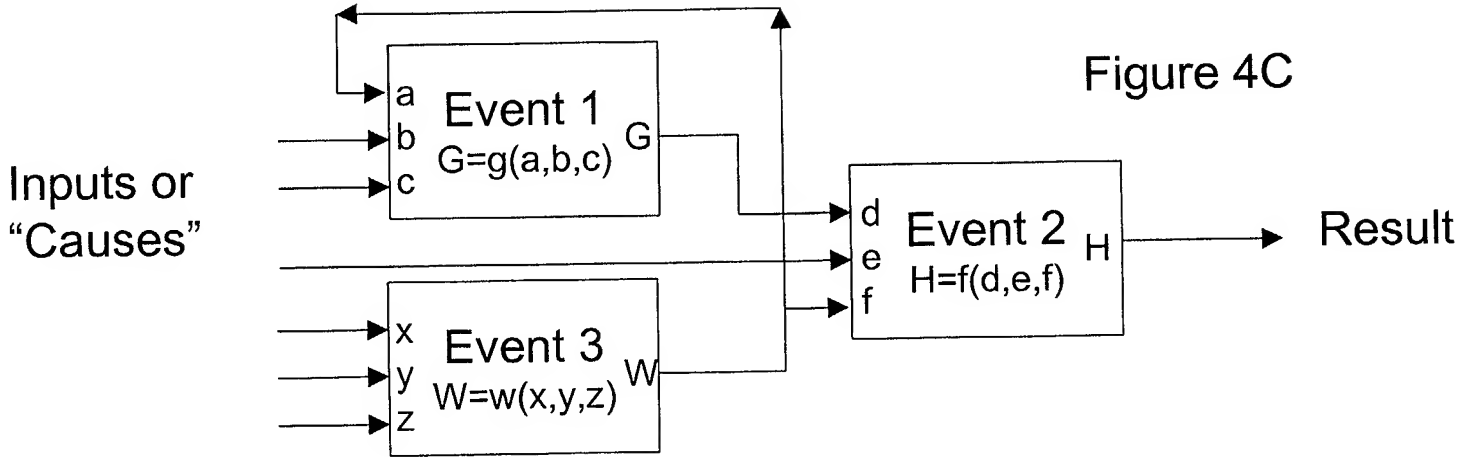
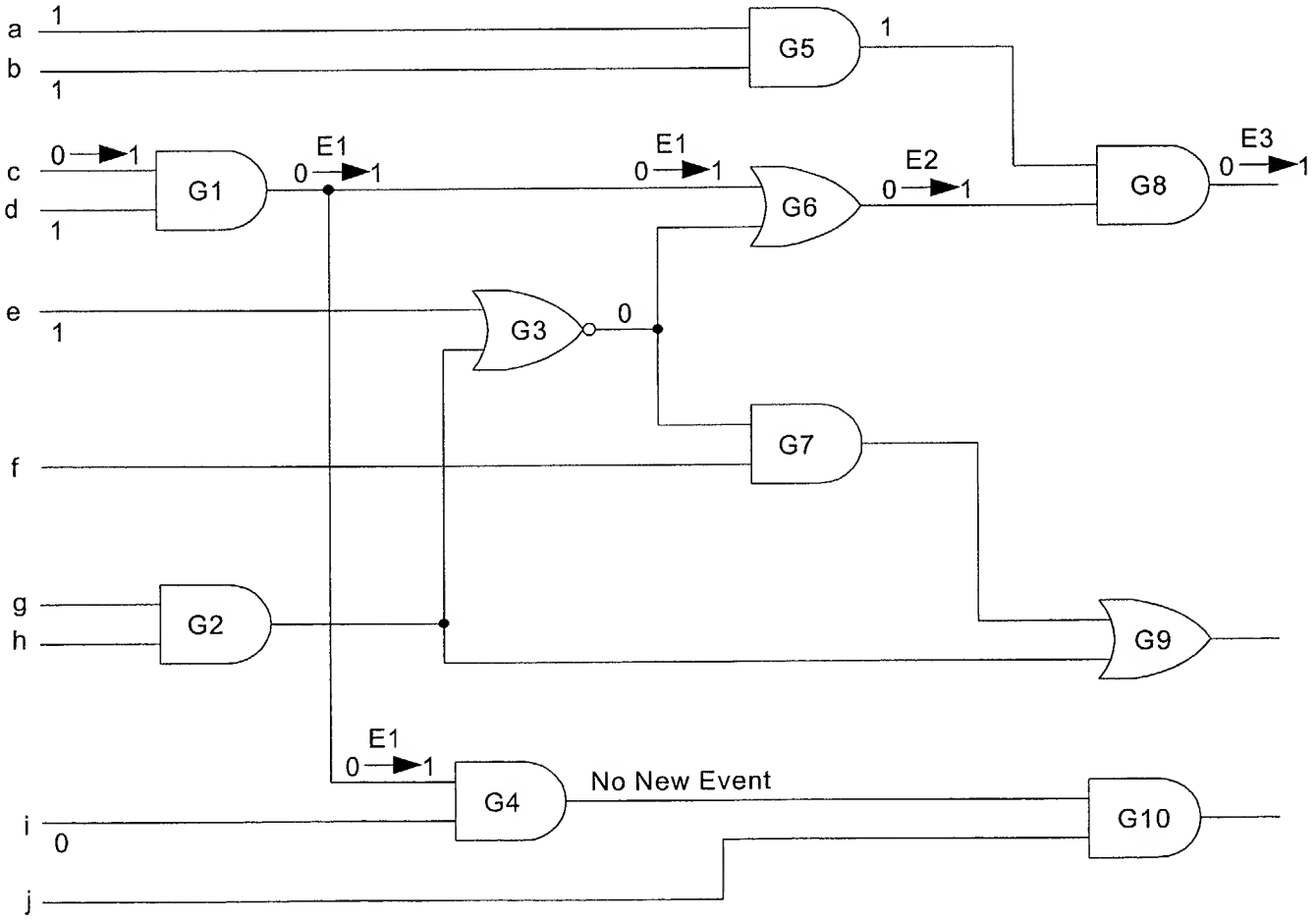


Figure 4C

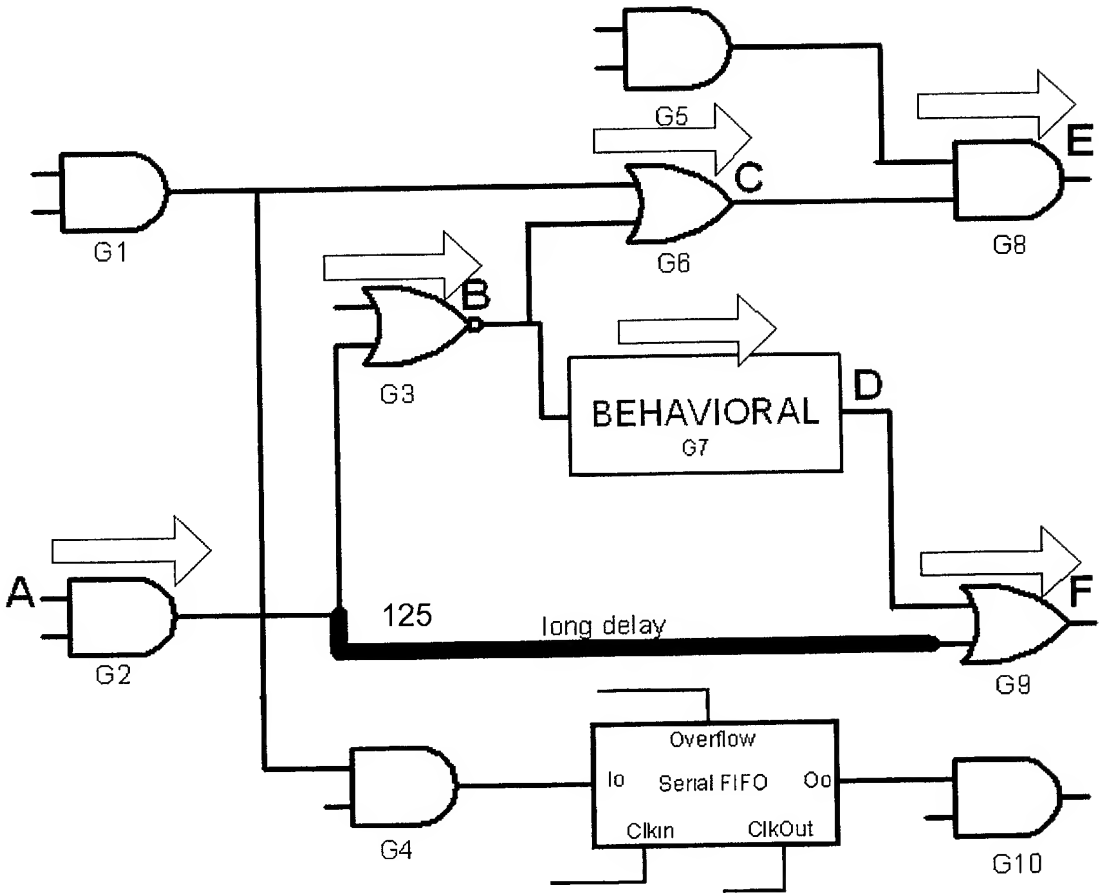
Conditional Event Topology

Figure 5A


a
b
c
d
e
f
g
h
i
j
1
1
1
0→1
1
1
0
1
0
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
E1
0→1
E1
0→1
E2
0→1
E3
0→1
No New Event

20TTE0" Z1E2A08T

Figure 5B



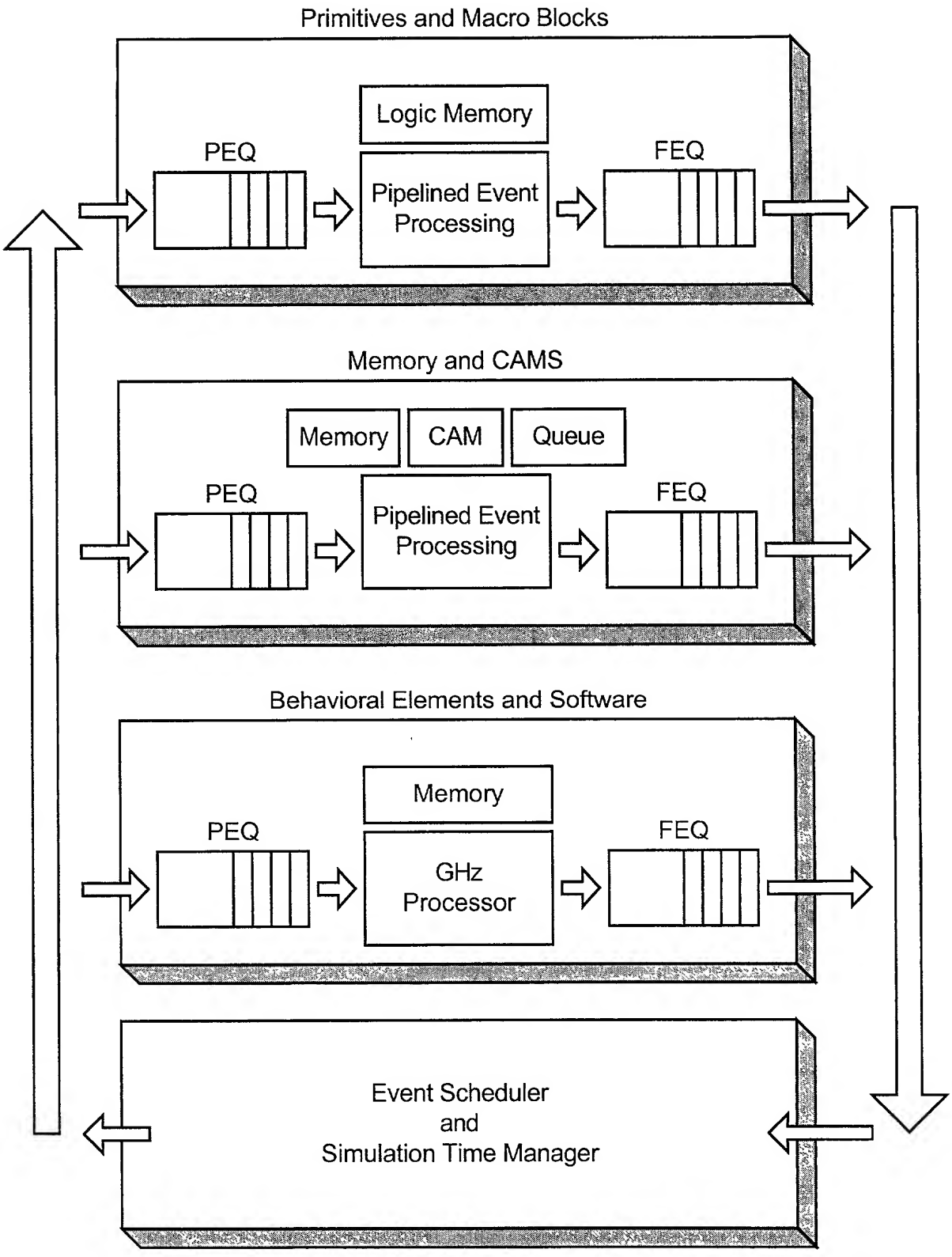

Primitives and Macro Blocks
Logic Memory
PEQ
Pipelined Event Processing
FEQ
Memory and CAMS
Memory
CAM
Queue
PEQ
Pipelined Event Processing
FEQ
Behavioral Elements and Software
Memory
PEQ
GHz Processor
FEQ
Event Scheduler and Simulation Time Manager

FIGURE 6

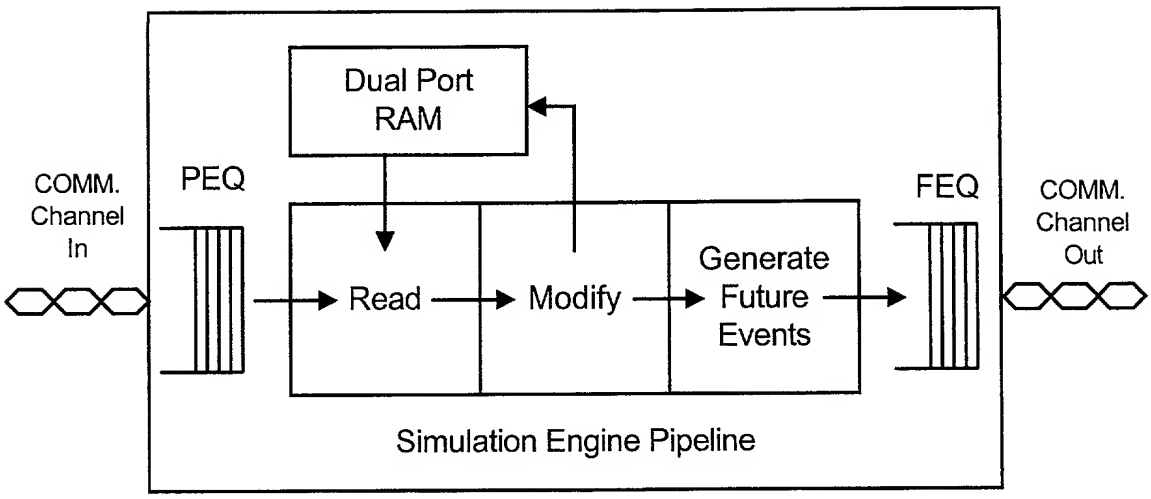
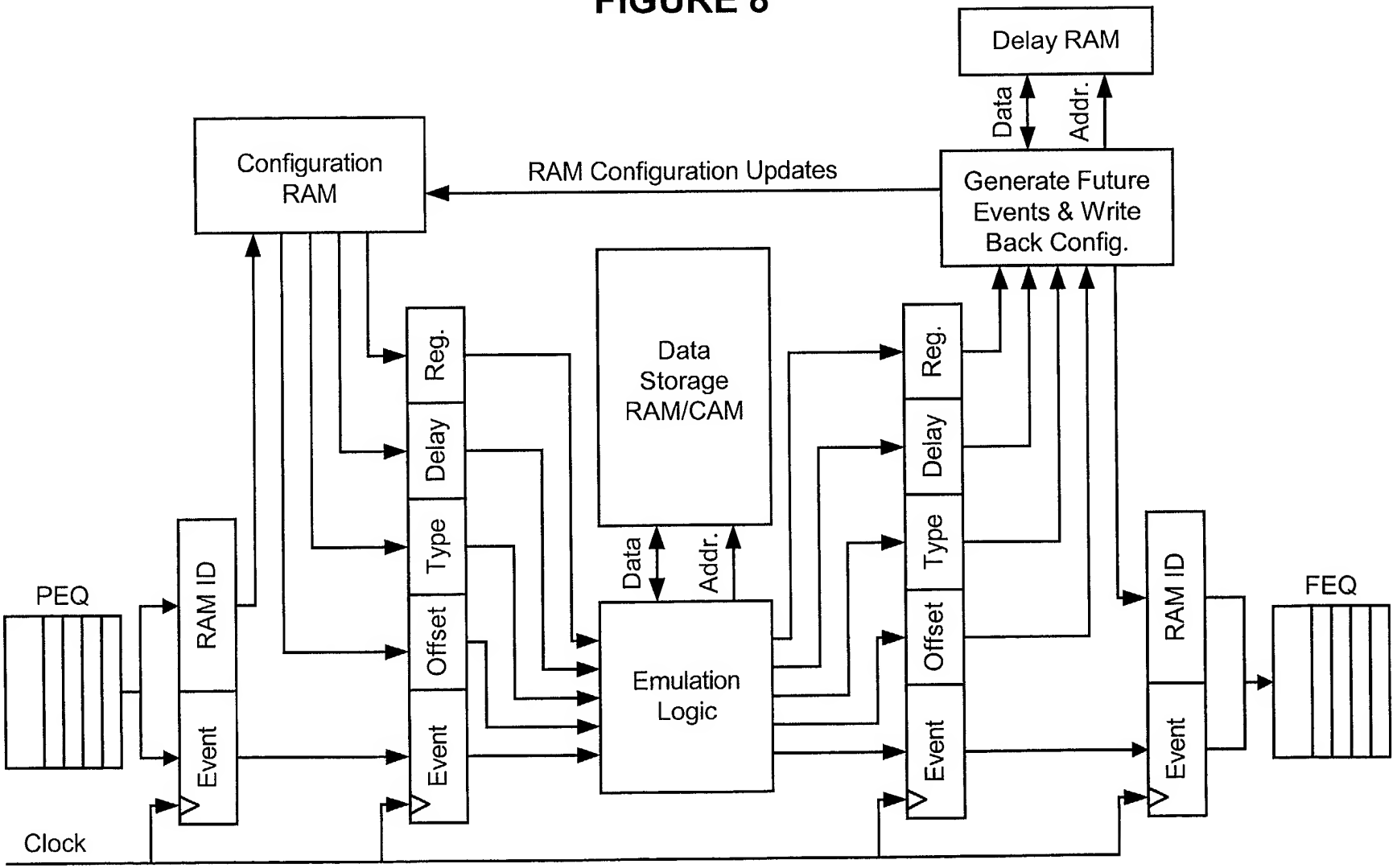

Dual Port
RAM
COMM.
Channel
In
PEQ
Read
Modify
Generate
Future
Events
FEQ
COMM.
Channel
Out
Simulation Engine Pipeline

FIGURE 7

FIGURE 8


Delay RAM
Data
Addr.
Configuration RAM
RAM Configuration Updates
Generate Future Events & Write Back Config.
Data Storage RAM/CAM
Reg.
Delay
Type
Offset
Event
RAM ID
PEQ
FEQ
Emulation Logic
Clock

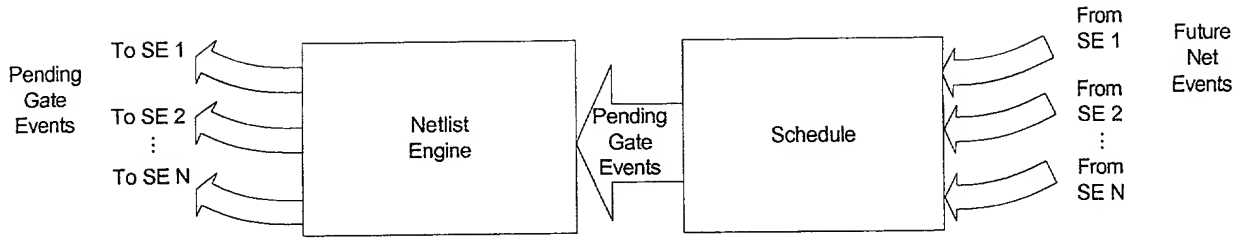


FIGURE 9A

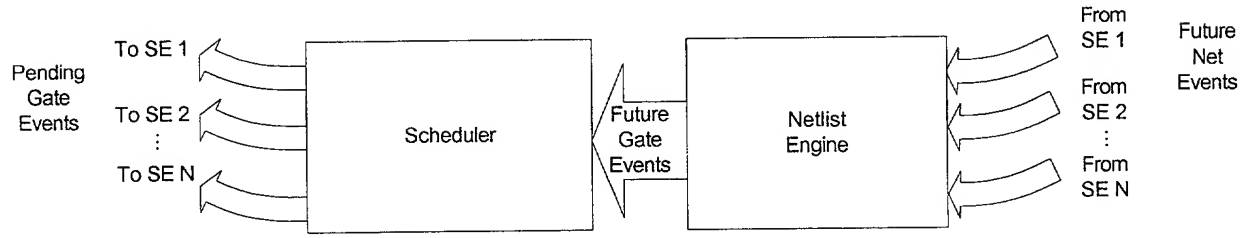


FIGURE 9B

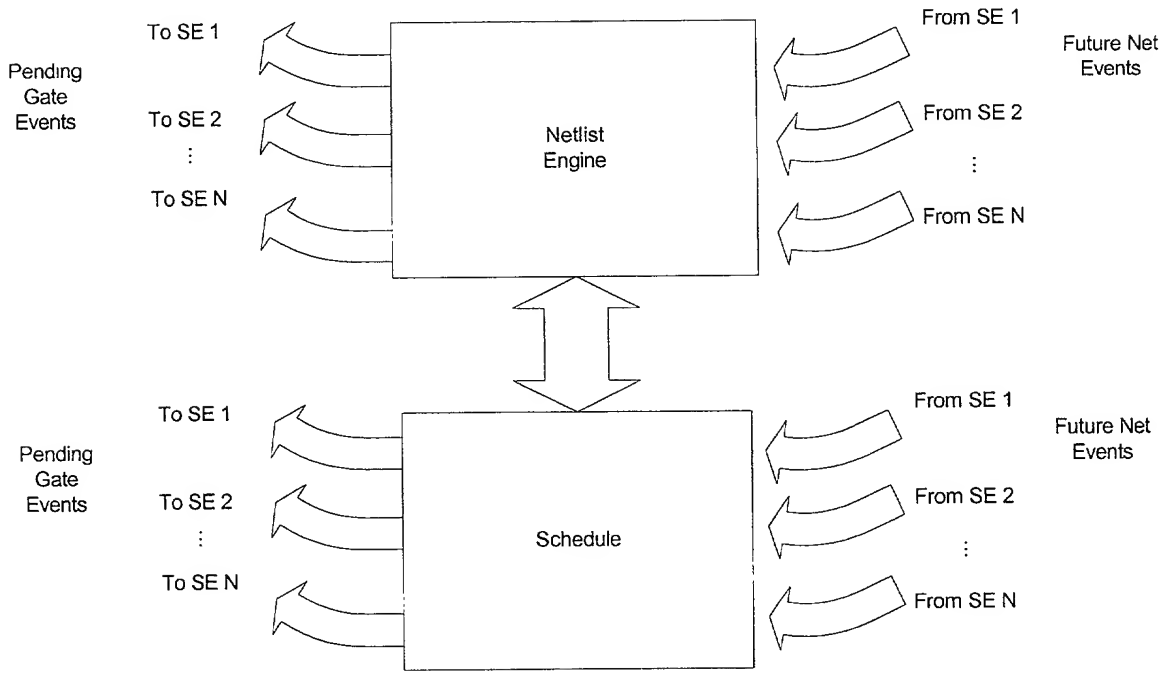


FIGURE 9C

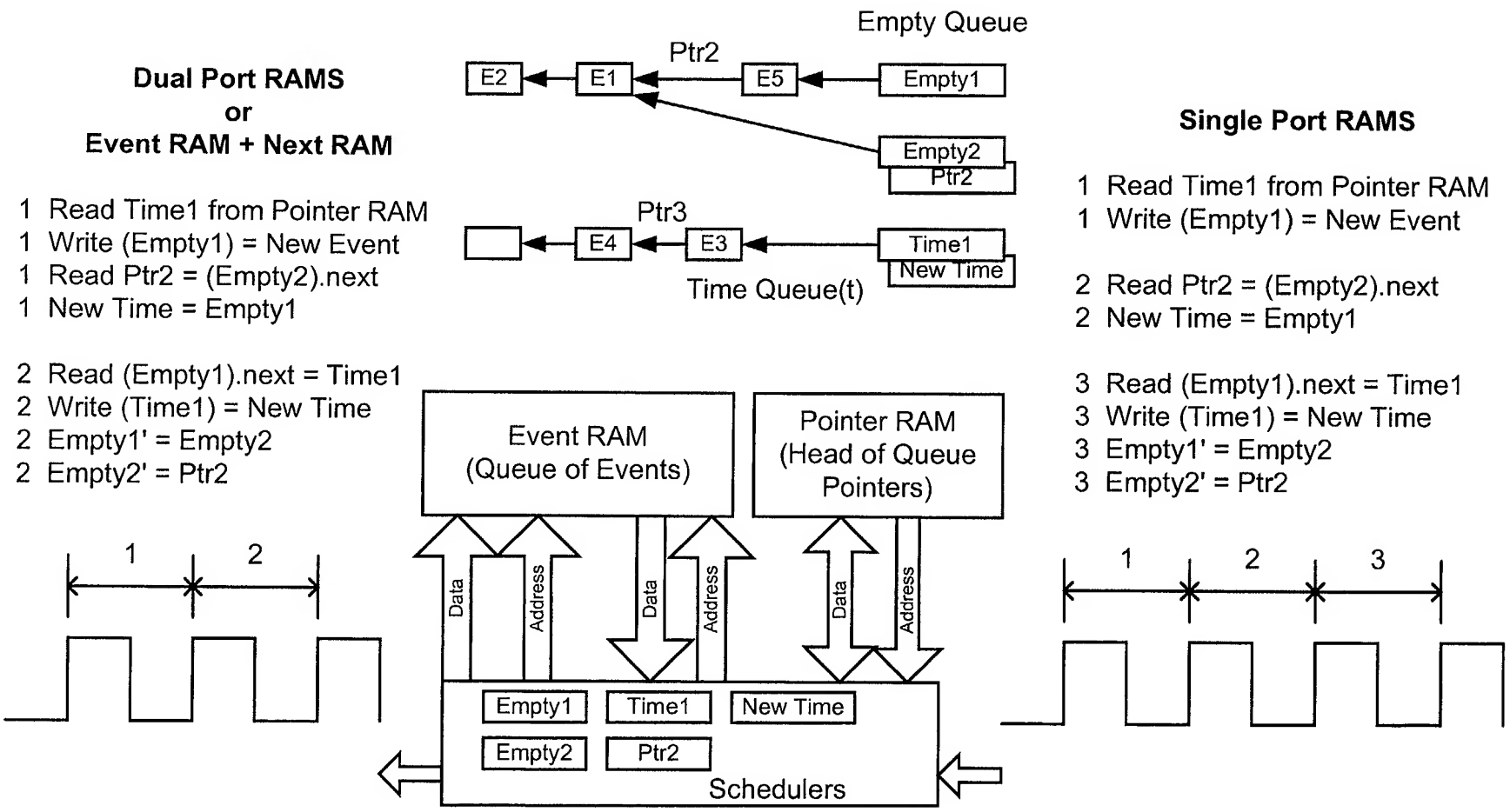

Empty Queue
Ptr2
E2
E1
E5
Empty1
Empty2
Ptr2
Ptr3
E4
E3
Time1
New Time
Time Queue(t)
Dual Port RAMS
or
Event RAM + Next RAM
1 Read Time1 from Pointer RAM
1 Write (Empty1) = New Event
1 Read Ptr2 = (Empty2).next
1 New Time = Empty1
2 Read (Empty1).next = Time1
2 Write (Time1) = New Time
2 Empty1' = Empty2
2 Empty2' = Ptr2
Event RAM
(Queue of Events)
Pointer RAM
(Head of Queue
Pointers)
Data
Address
Data
Address
Data
Address
Empty1
Time1
New Time
Empty2
Ptr2
Schedulers
1
2
Single Port RAMS
1 Read Time1 from Pointer RAM
1 Write (Empty1) = New Event
2 Read Ptr2 = (Empty2).next
2 New Time = Empty1
3 Read (Empty1).next = Time1
3 Write (Time1) = New Time
3 Empty1' = Empty2
3 Empty2' = Ptr2
1
2
3

FIGURE 10

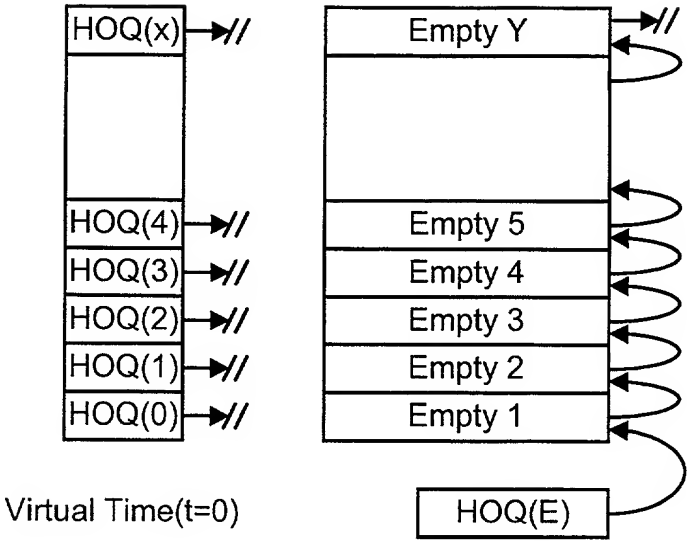


FIGURE 11A

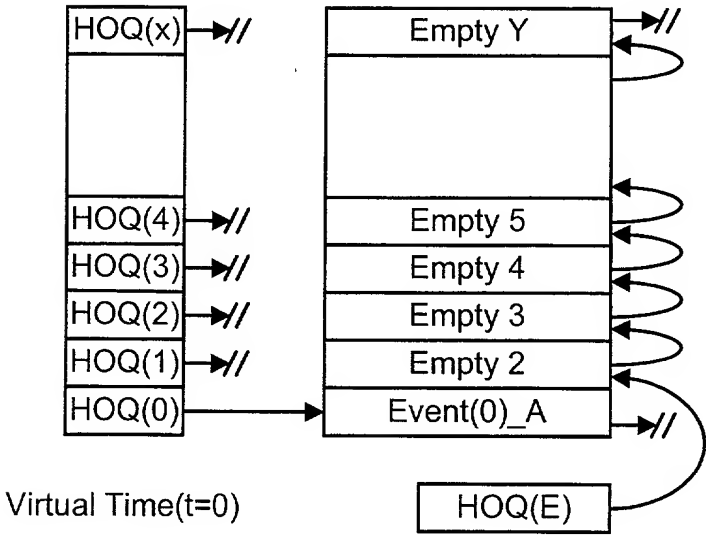


FIGURE 11B

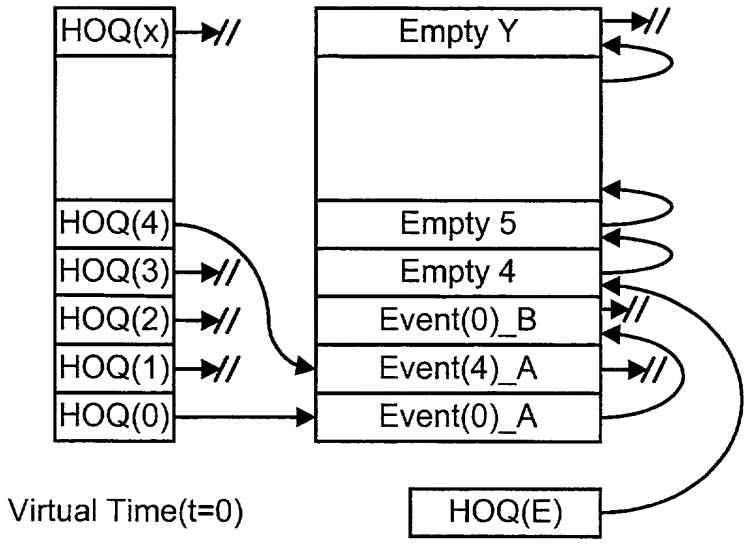


FIGURE 11C

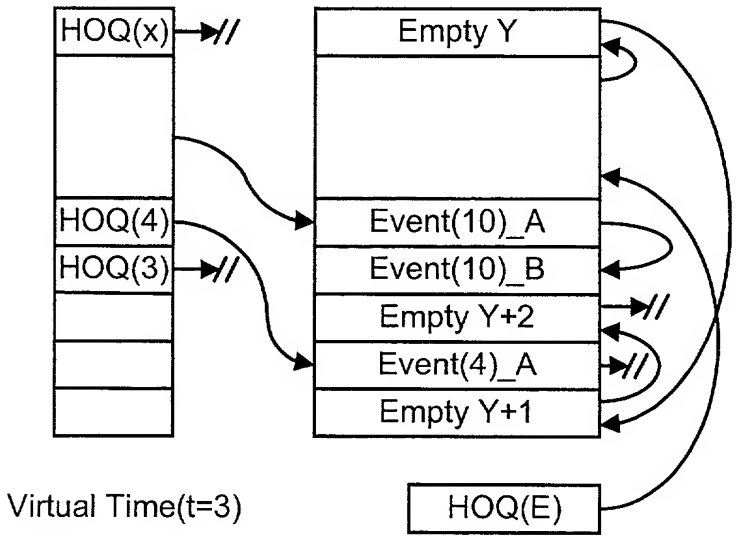
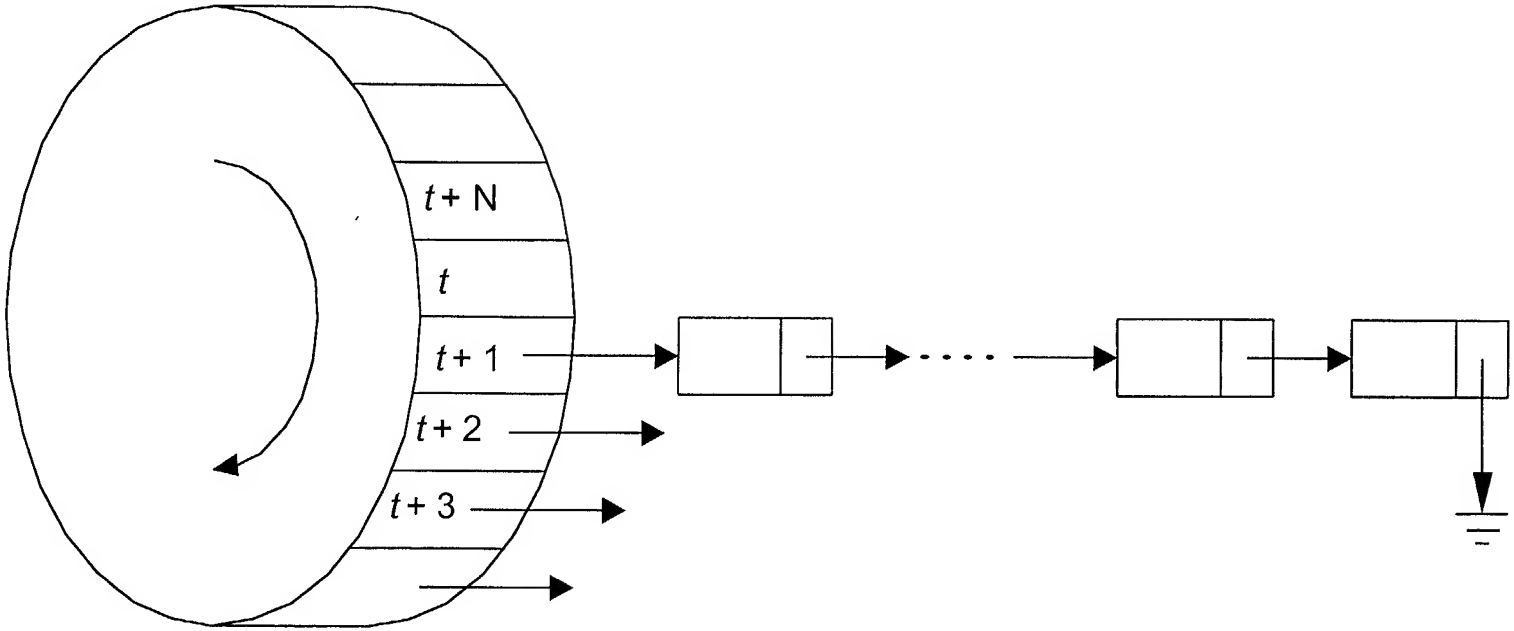


FIGURE 11D

FIGURE 12



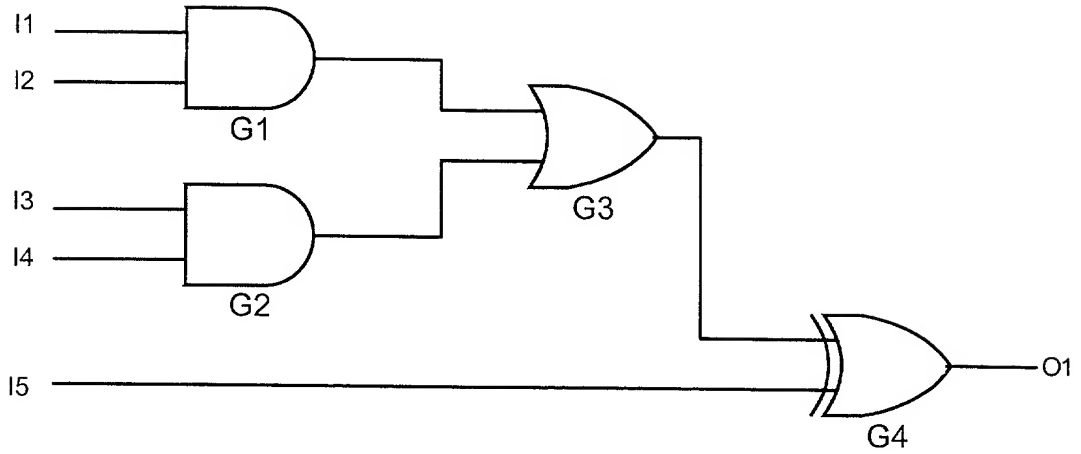


FIGURE 13A

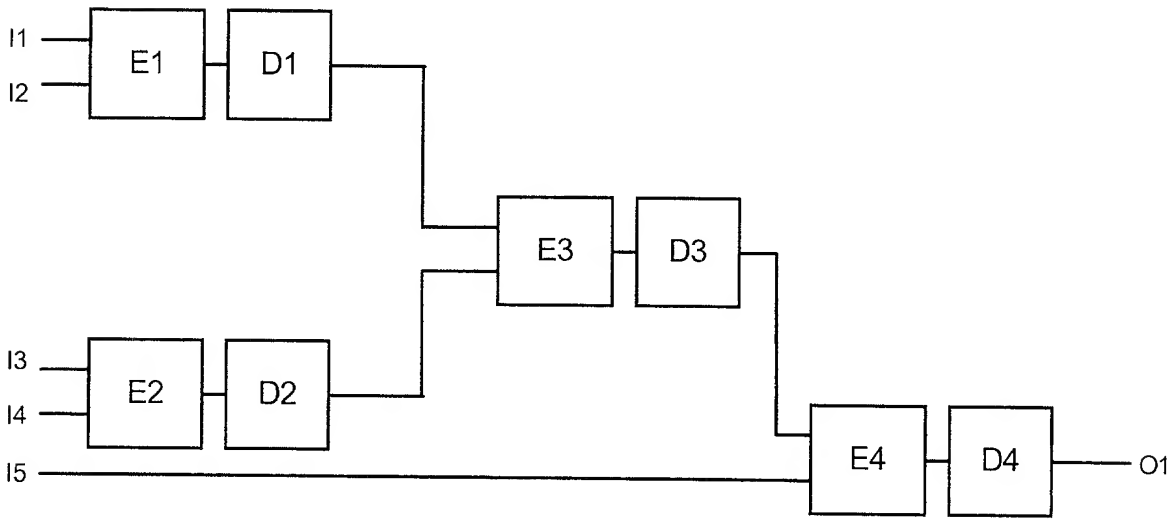


FIGURE 13B